ABSTRACT

Ferroelectric memory cells and fabrication methods are provided in which the memory cell comprises a ferroelectric capacitor in a capacitor layer above a semiconductor body, and a cell transistor with first and second source/drains formed in an active region of the semiconductor body. The active region extends along a first axis in the semiconductor body, and the cell includes a gate electrically coupled with a wordline structure that extends along a second axis, wherein the first axis and the second axis are oblique.